UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,575	02/24/2004	Tomasz Kaczynski	499.754US1	9879

21186 7590 09/13/2007

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
PATEL, KAUSHIKKUMAR M	

ART UNIT	PAPER NUMBER
2188	

MAIL DATE	DELIVERY MODE
09/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

mm

Office Action Summary	Application No.	Applicant(s)	
	10/785,575	KACZYNSKI, TOMASZ	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-22,24,25,35-39 and 41-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-22, 24, 25, 35-39 and 41-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed May 24, 2007 in response to PTO Office Action mailed December 21, 2006. The applicant's remarks and amendments to the claims and/or specification were considered with the results that follow.

2. In response to last Office Action, claims 1-3, 7, 10, 13, 17-22, 24, 35-39 and 41 have been amended. Claims 4, 23, 26-34 and 40 have been canceled. Claims 43-45 have been added. As a result, claims 1-3, 5-22, 24, 25, 35-39 and 41-45 remain pending in this application.

Response to Arguments

3. Applicant's arguments filed May 24, 2007 have been fully considered but they are not persuasive.

Applicant amended specification to overcome rejection of claims 35-42 under 35 U.S.C. 101, but the amended specification still refers to tangible and intangible embodiments ("machine-readable media includes any mechanism that provides (i.e. stores and/or transmits) information"). Also, applicant has not explicitly disavow the canceled matter from the specification and hence the original specification still has support for both the tangible and intangible subject matter for the machine-readable media, thus the rejection of claims under 35 U.S.C. 101 maintained.

Applicant argues that his ISDS can determine two or more cells each of which indicates a corresponding system cache having a copy of a memory without the need of bit-vector information (remarks, pages 16 and 17). Although, the claim 1 recites the limitation "wherein requesting includes transferring to the ISDS bit-vector information associated with the evicted ISDC entry" (claim 1, lines 24-25), thus applicant's arguments are not persuasive.

Applicant argues "Michael does not teach or suggest how each entry of the cache directory keeps track of a copy of a given local memory line cached in a plurality of system caches throughout multiple nodes (see e.g. Fig. 8)". The examiner was unable to find the relationship of argument with the claimed invention, because no claim claims such limitation, the system cache is not equivalent to caches in different nodes, because having one node with multiple cache is enough to fulfill the requirements of the claim. Further, the fig. 8 of the Michael is directed to uniprocessor or single processor system and is the one of the multiple embodiments. Figure 1 of the Michael teaches multi-node system, where the directories keeps the track of a copy of a given local memory line (see, Michael, pars. [0002] – [0003]).

Applicant argues that cited paragraphs of Joseph (US 6,405,292) and Carpenter (US 6,266,743) do not teach all the limitations, i.e. in case of cache miss putting the request in the pending buffer and do not teach storing operation request into pending queue but instead teaches storing memory address and state information or status information of memory transaction in progress. With respect applicant's arguments it is noted that the paragraph numbers or line numbers cited in the rejection were for

applicant's convenience, however the actual rejection is based on entire document and not only on cited passages. Joseph teaches a coherence controller with pending buffer, which is separate from the cache as applicant argues (Joseph, figs. 1 and 2). According to Joseph, the coherence controller includes directory controller and pending buffer, the directory controller performs the lookup with respect to cached lines in the system and receives the state information of the memory line (i.e. transaction) and puts the request waiting for information (i.e. state information) into the pending buffer (Joseph, col. 3, line 40 – col. 5, line 33), where it is readily apparent to one having ordinary skill in the art, the placing request/response waiting for data and/or coherency/state information into to pending buffer allows the next request to be processed, the concept is known in the art as non-blocking processing, thus according to broadest reasonable interpretation, using pending buffer provides faster memory accessing and thus increasing the speed of the system. Thus, Joseph is relied upon to teach a pending buffer, where it is readily apparent to one having ordinary skill in the art that in system of Michael, when there is directory cache miss, the operation request that caused a miss awaits (i.e. pending) data reply from memory directory and Joseph teaches placing such requests/responses into pending buffer allows starting next operation request as well as determining of collision between transactions, while the pending operation awaits data from directory. Similarly, Carpenter also provides coherence controller, which stores indication of the system memory addresses of data (e.g. cache lines) checked out to caches into remote nodes (Carpenter, col. 8, lines 10-14). Carpenter further teaches use of eviction buffer (i.e. similar functionality as of pending buffer), which keep track of the memory requests

that is being evicted from the system caches. With respect to applicant's arguments about only keeping status information of the operation, applicant's own directory cache and directory storage performs the same functions (i.e. keeping state information only) (*"one embodiment the apparatus includes the Ingrained Sharing Directory Storage (ISDS) to store state information about copies of local memory lines whose directory entries were evicted from the ISDC, wherein the ISDS includes a first set of cells, wherein each cell contain plurality of entries, wherein each entry can contain state information about a copy of a local memory line and wherein each entry does not contain state information about a copy of a remote memory line"*, see present application specification, page 4, lines 2-8. *"In one embodiment, to improve performance of an ISD scheme, the coherence buffers can be partitioned. Each partition of a coherence buffer may have a separate ISDS, ISDC, and it would maintain state for local memory lines cached in a subset of system caches"*, see present application specification, page 14, lines 1-4).

Applicant argues that Joseph-2 (US 6,338,123) separate shadow directory. The examiner respectfully disagrees with the fact. According to Joseph-2, the CCR directory is a 64-way system using 8-way nodes per coherence controller (Joseph-2, col. 3, lines 37-40). Applicant further argues that it is not clear how CCR directory determines a shadow directory. As per Joseph-2, the CCR directory keeps state information on memory lines belonging to local memory that are cached in remote nodes and it is done by keeping shadow of each shared cache directory or remote directory (col. 3, lines 30-35). The concept of shadowing is well known in the art and means "copy of original",

hence it is readily clear that the CCR keeps copies of each remote cache directory. This is also evident from Joseph-2 at col. 4, lines 1-12, "the degree of associativity of the shadow directory in the CCR is same as the degree of associativity of the corresponding remote cache".

Applicant's remaining arguments are directed towards prior art not teaching limitations of amended claims and thus it is addressed below with respect to the rejection of claims.

Claim Objections

4. Claim 5 is objected to because of the following informalities:

Claim 5 depends from canceled claim 4 instead it should depend on claim 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

6. Claims 1-2, 18-21 and 35-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 18 and 35 recites the limitation "wherein the indication is extracted from two or more ISDS entries matching the incoming memory address" in lines 6-7, 11-12 and 12-13 respectively. The limitation is not true in all conditions, such as only one

cache is caching the requested data or none of the caches has the data (in this condition only one entry matches or no entry matches), thus the limitation "two or more entry matching" renders the claim indefinite. (Due to ambiguities describe above the limitation is interpreted as "the indication is extracted from any number of matching entries" (i.e. none, one or more etc.).

Claims 2, 19-21 and 36-38 are also rejected due to dependency on rejected claims.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 35-39, 41 and 42 are rejected under 35 USC 101, because claims are not limited to tangible embodiments. In view of applicants' disclosure, specification page 8, line 21 to page 9, line 3, the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g. ROM, RAM, magnetic/optical storage medium etc.) and intangible embodiments (e.g. mechanism that transmits the information). As such, the claims are not limited to statutory subject matter and are therefore non-statutory.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-3, 5, 7, 9-22, 24, 35-39, 41 and 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michael et al. (US 2002/0002659 A1), Joseph et al. (US 6,405,292), Carpenter et al. (US 6,266,743), Joseph et al. (US 6,338,123) (Joseph-2 herein after) and Lilja et al. (A Superassociative Tagged Cache Coherence Directory, submitted by applicant as an IDS on 2/24/2004, with publication date of October 10, 1994).

As per claim 1, Michael teaches a method comprising:

receving in an ingrained sharing directory cache (ISDC) an incoming operation request including an associated incoming memory address (Michael, pars. [0019], [0033], [0035], taught as receiving, in the directory cache (DC), a disk or memory request, memory request inherently requires associated address);

determining if the incoming operation is an ingrained sharing directory storage (ISDS) data reply, wherein the ISDS data reply includes an indication of system caches storing a memory line having the same memory address as the incoming address (Michael teaches receiving a memory access request, than controller performs directory cache lookup and if miss occurs during the lookup, the request is sent to directory storage for further information and the directory storage sends a data reply (ISDS data reply) back to directory cache with the necessary information (indication of who shares the data and if the data is valid, invalid etc.), where it is readily apparent to one having ordinary skill in the art that the system must determine whether the incoming operation

is a data access request or it is a data reply, because both the request and reply are sent to the controller, Michael, pars. [0035], [0036]);

completing a pending ISDC entry if the incoming operation request is an ISDS data reply, wherein completing includes locating a pending ISDC operation associated with the ISDS data reply (as explained above when the incoming operation, i.e. request to access data is sent from processor, the DC lookup is performed and if there is miss, the controller requests data from memory directory and during the time while data is being retrieved from the memory directory, the operation waits for the requested data (i.e. pending operation) and when the information is received from memory directory (i.e. data reply), the controller finds the pending memory request and completes the pending operation associated with data reply (i.e. the request that caused the miss in the DC));

if the incoming operation request is not an ISDS data reply and if there is an ISDC entry associated with the incoming operation request, performing the incoming operation request (Michael, par. [0035], "if there is a hit in the DC, the corresponding directory information is read", as explained above the controller must determine whether the incoming operation is a data request or data reply); and

if the incoming operation request is not an ISDS data reply and if there is no ISDC entry associated with the incoming operation request, creating an ISDC entry if there is no ISDC entry associated with the incoming operation request (Michael, par. [0035], "if a hit is not detected, the requested information is acquired from the memory

directory", again as explained above the controller must determine whether the incoming operation is a data request or data reply); wherein creating includes:

requesting information associated with the incoming memory address from the ISDS (Michael, par. [0035], "if a hit is not detected, the requested information is acquired from the memory directory", par. [0036], teaches address);

evicting another ISDC entry if there is no free ISDC entry; wherein the evicting includes: requesting the ISDS to store the information the evicted ISDC entry (Michael, par. [0032], the information is written back into the memory directory, par. [0036], if none of the ways is invalid (i.e. no free entry), one of them is selected and its contents are written to the memory directory); designating the evicted ISDC entry to the incoming request (Michael, par. [0036], one entry is selected and its contents are written to the memory directory, and replaced by the new tag and the directory entries from the memory directory).

Michael fails to teach that indication is extracted from two or more matching entries. Lilja teaches a superassociative tagged cache structure, where the multiple entries can match to a single address ("an a-way superassociative tagged directory allows up to a tags in a set to have the same address value", Lilja, page 2, fig. 2, sec. 2). It would have been obvious to one having ordinary skill in the art at the time of the invention to use superassociative tagged cache as taught by Lilja in the system of Michael to reduce premature invalidation of cache lines from caches (Lilja, page 1, right col.).

Michael teaches the incoming operation request waits (pending) for data from memory directory but fails to teach pending buffer as required by claim. Joseph teaches pending buffer used by coherent controllers (Joseph, col. 1, lines 21-67) and Carpenter teaches eviction of cache entry using pending buffer (Carpenter, col. 8, lines 28-55). Joseph and Carpenter both teach that pending buffers maintains the status of memory transactions in progress and means for detecting collisions if there is another request for same entry (Joseph, col. 1, lines 14-20, col. 3, line 40 – col. 4, line 33, Carpenter, col. 8, lines 50-55). Thus, it would have been obvious to one having ordinary skill in the art at the time of the invention to use pending buffer as taught by Joseph and Carpenter in the system of Michael and Lilja to maintain coherency while transaction is in state of transition avoiding collisions (Joseph, col. 1, lines 14-20, col. 3, line 40 – col. 4, line 33, Carpenter, col. 8, lines 50-55).

Michael, Joseph, Carpenter and Lilja fail to teach, dynamic full map of memory lines as required by claim 1. Joseph-2 teaches dynamic full map directory keeping track of state information of memory lines cached in system caches (Joseph-2, col. 2, lines 17-49). It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize dynamic full map directory as taught by Joseph-2 in the system of Michael, Joseph, Lilja and Carpenter to improve system performance with simple coherence protocol (Joseph-2, col. 2, lines 12-15). Joseph-2 teaches multi-way dynamic full map directory, which maintains state information of local lines cached in remote caches by each way for each remote cache (Joseph-2, col. 3, lines 14-60). Joseph-2 also teaches extracting bit-vector information (Joseph-2, col. 4, lines 35-55).

With respect to remaining limitations, such as locating pending operation in the pending queue and making evicted entry pending, Joseph teaches putting a memory request in pending buffer during memory transaction in progress, i.e. in case of directory cache miss in the system of Michael, the request is waiting for data from memory directory is stored in the pending buffer (Joseph, col. 1, lines 14-67, col. 3, line 40 – col. 4, line 33). Carpenter teaches that selected eviction entry is placed in eviction buffer (pending buffer) and generated proper interconnect transactions (getting information from memory directory. Michael teaches that if memory tag does not match (miss), the controller request necessary information from memory directory, Michael, par. [0036]). Replacing a cache line from memory directory is a memory transaction in progress and it would have been obvious to one having ordinary skill in the art at the time of the invention to put in eviction buffer (pending buffer) as taught by Carpenter to maintain the coherency. Checking status of pending entry with respect response is inherent in the system of Joseph and Carpenter.

As per claim 2, Carpenter teaches different kinds of memory lines states such as Modified, shared, exclusive etc. (Carpenter, col. 4, lines 30-35, col. 7, line 50-67).

As per claims 3 and 5, Michael, Joseph, Lilja and Carpenter teach receiving a directory storage request; and selecting an entry in an ISDS from plurality of entries (see rejection of claim 1 above).

Michael, Joseph, Lilja and Carpenter fail to teach, dynamic full map of memory lines as required by claim 3. Joseph-2 teaches dynamic full map directory keeping track of local memory lines in remote caches (Joseph-2, col. 2, lines 17-49). It would have

been obvious to one having ordinary skill in the art at the time of the invention to utilize dynamic full map directory as taught by Joseph-2 in the system of Michael, Joseph and Carpenter to improve system performance with simple coherence protocol (Joseph-2, col. 2, lines 12-15). Joseph-2 teaches multi-way dynamic full map directory, which maintains state information of local lines cached in remote caches by each way for each remote cache (Joseph-2, col. 3, lines 14-60).

With respect to remaining limitations of claim 3, such as the structure of directory storage corresponding to remote and local caches (number of buffer equals to number of cache sets in remote and local caches) as well as cache structure such as direct or associative or set-associative, number of sets of directory, number of entries per sets etc. are not explicitly taught by Michael, Joseph, Carpenter and Joseph-2, but such information is merely a matter of design choice and would have been obvious in the system of Michael, Joseph, Carpenter and Joseph-2. These limitations fail to define a patentably distinct invention over Michael, Joseph, Carpenter and Joseph-2, since both the invention as a whole directed to maintaining dynamic full map of local memory lines in caches in remote system caches (Joseph-2 however teaches similar structure, Joseph-2, col. 3, lines 38-50, fig. 4).

Michael and Joseph-2 teach set-associative directory cache and respective request formation, including tag, set ID, offset and state of the memory line (Michael, figs. 5-6, Joseph-2, fig. 4), thus depending upon the structures of cache and directories (as explained with respect to claim 3 above) it is inherent to include SELECT_CB field,

SELECT_CELL field and MEMORY_TAG field for selection of respective buffer and further respective cell from buffer.

As per claim 7, Michael teaches coherence controller controlling operations with respect to system caches and directory cache as well as memory directory. Directory cache stores the information about memory lines cached in system caches (Michael, fig. 3, par. [0031]). Lilja teaches matching plurality of entries to address tag (see claim 1 above). Joseph, Carpenter and Joseph-2 teach pending queue and dynamic full map directory as explained with respect to claims 1 and 3 above.

As per claim 9, Michael teaches caches having set-associative structure (Michael, par. [0033]).

As per claim 10, Michael, Joseph, Lilja and Carpenter teaches directory cache (Michael, fig. 4) to store state information about recent copies of local memory blocks (Michael, par. [0008]), the directory cache to receive directory storage requests and create directory cache entries from information presented by the directory storage (explained with respect claims 1 and 3, above); and

a directory cache pending queue to store pending operations (Joseph and Carpenter teach this limitation as explained with respect to claim 1 above). Lilja teaches plurality of entries with address tag and Joseph-2 teaches dynamic full map directory (see claims 1 and 3 above).

Claim 11 is rejected under same rationales as applied to claim 2 above.

As per claim 12, Michael teaches writing state information to memory directory (Michael, par. [0032] and retrieving information from directory (pars. [0035]-[0036]), which inherently teaches fetching or modifying state information.

Claims 13-16 recites limitations, including number of nodes in the system, each node having number of set-associative caches (Michael, fig. 3, item 310), a directory storage having number of buffers and each buffer having some number of cells and cells with directory entries. All the limitations above are rejected under same rationales as applied to claim 3 as design choice and would have been obvious in the system of Michael, Joseph, Carpenter, Lilja and Joseph-2.

As per claim 17, Michael teaches main memory unit (Michael, fig. 3, item 330), which is a random access memory.

Claims 18-20 are similar in scope with respect to claim 1 and hence rejected under same rationales as applied to claim 1.

As per claim 21, Michael teaches directory cache and memory directory with state information indicating which cache(s) has a copy of the memory line (Michael, par. [0002]), which inherently teaches how many (only one or more or none) copies of memory line is present in the system. With respect limitation, wherein the memory line is located at the memory address, is inherent in order to work system error free.

Claims 22, 24, 39, 41 and 43-45 are rejected under same rationales as applied to claims 1-3, 5 and 10-12 above.

Claims 35-38 are similar in scope with respect to claims 18-21 above and hence rejected under same rationales as applied to claims 18-21 above.

11. Claims 6, 8, 25 and 42 are rejected under **35 U.S.C. 103(a)** as being unpatentable over Michael et al. (US 2002/0002659 A1), Joseph et al. (US 6,405,292), Carpenter et al. (US 6,266,743), Joseph et al. (US 6,338,123) (Joseph-2 herein after) and Lilja et al. (A Superassociative Tagged Cache Coherence Directory, submitted by applicant as an IDS on 2/24/2004, with publication date of October 10, 1994) as applied to claims 3, 7, 22 and 39 above and further in view of Lai (US 5,564,035).

As per claims 6, 8, 25 and 42, Michael, Joseph, Carpenter, Lilja and Joseph-2 teach all the limitation of parent claims but fail to teach memory line residing only in one buffer or combination of ISDC set and ISDS set combined includes all copies of memory lines cached at any point in time. Lai teaches concept of caches having non-inclusive configuration, which teaches limitation memory line residing only in one buffer or total of all sets includes all copies of memory lines at any point in time (Lai, col. 3, lines 24-35). It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize non-inclusive cache levels as taught by Lai in the system of Michael, Joseph, Carpenter, Lilja and Joseph-2 to increase the efficiency of caches and thus reducing adjacent level cache sizes (Lai, col. 3, lines 1-20).

Conclusion

12. The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

13. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
9/11/07